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# Reliability of Power GaAs FET's—Au Gates and Al–Au Linked Gates

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**Abstract**—An investigation of the reliability of two types of commercial microwave power GaAs FET's has been carried out. Mean-time-to-failure data for a device mounted face-up with Al gates but without an Al–Au couple is presented and similar data for a "flip-chip" mounted Au-refractory gate device is reviewed. The failure mechanisms for both devices are described.

## I. INTRODUCTION

FOR SOME TIME, the Naval Research Laboratory (NRL) has been engaged in assessing the reliability of power GaAs FET's [1], [4]. The devices discussed in this paper were selected for evaluation for two reasons: 1) they are commercially available; and 2) they represent two different approaches to obviating a "gate void" problem [1]–[3] which occurs in devices with direct coupling between Al gate pad and Au. Such devices have very short mean-time-to-failures (MTTF's) as has been reported previously [1].

A causal relationship has now been established between the Al–Au couple and void formation [1]–[3]. There are at least two solutions to this problem: 1) the use of Au-refractory gates; 2) the Al gate in combination with a refractory link so that Au and Al do not come in contact. The Microwave Semiconductor Corporation (MSC) has

chosen the first while Raytheon has chosen the second solution. Unfortunately, in the case of the Raytheon device, the "solution" has introduced a new failure mechanism. However, in both cases, the void problem does not appear as a failure mode.

Both types of devices tested, Raytheon LNC 832D FET's and MSC 88002 FET's, are fabricated on semi-insulating GaAs substrates with buffer layers between the substrate and active layer. They both also have ohmic contacts formed by depositing Au–Ge/Ni on an  $n^+$  layer. The Raytheon devices have one center-fed  $1 \times 500 \mu\text{m}$  Al gate stripe and produce a nominal power output of approximately 200 mW at X-band. A refractory barrier metal sandwich has been fabricated between the Al gate and Au bonding pad to eliminate a direct Al–Au connection.

The MSC devices have eight titanium–tungsten–gold (Ti–W–Au) gate stripes, each of  $1 \times 150\text{-}\mu\text{m}$  dimensions and yield a nominal 0.5 W of output power at X-band. These FET's are mounted in a "flip-chip" configuration. All of the Raytheon FET's and most of the MSC devices tested were supplied in delidded packages although a few of the MSC units were mounted in packages with covers.

## II. TEST CONDITIONS

Before the devices were subjected to temperature accelerated life testing under RF conditions, a number of dc parameters were measured. These always included the normal grounded source transfer characteristics. In addition, gate-source current–voltage ( $I$ – $V$ ) characteristics were always measured. The latter proved to be the best indication of physical changes in the devices under test.

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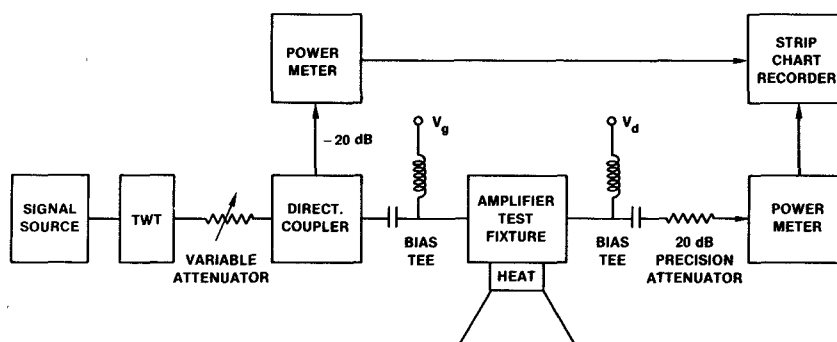


Fig. 1. Test apparatus for microwave frequency accelerated stress testing.

The equipment used for the accelerated testing is shown in Fig. 1. Devices were operated at 8 GHz in single-stage MIC amplifier test fixtures designed by their manufacturers. For the Raytheon devices, sliding double slug tuners manufactured by Alford were used at the input and output of the MIC fixtures to optimize power input and output. In general,  $V_{ds}$  (drain-source voltage) was set to 8–10 V and  $V_{gs}$  (gate-source voltage) was optimized for maximum power output at room temperature. An RF power input of 40 mW was selected for the Raytheon devices and 100 mW for the MSC devices. This was sufficient to produce amplifier operation in the saturated region.

During testing, the following parameters were continuously monitored: RF power input, RF power output, gate current, drain current, drain-source voltage, gate-source voltage, and base-plate temperature. Noncatastrophic failure was arbitrarily defined as a 1-dB decrease in power output at room temperature.

### III. DETERMINATION OF CHANNEL TEMPERATURE

Channel temperature was not measured for each device, but instead was estimated from measurements of thermal resistance as a function of temperature on typical devices using the electrical method [5]. This method makes use of the linear relationship between forward gate-source voltage and temperature (for a constant gate current) which is characteristic of Schottky barrier diodes. It is the only satisfactory method of determining thermal resistance when the surface of the device is inaccessible.

A thermal resistance of between 95–110°C/W was measured for the Raytheon devices and a thermal resistance of between 25–30°C/W was measured for the MSC devices with each device under test mounted in the same holder (amplifier) as used for the accelerated stress testing. The measurement thus reflects the total channel to ambient thermal resistance in the RF mount, and *not* the channel to package case thermal resistance.

### IV. ACCELERATED TEMPERATURE STRESS RESULTS AND FAILURE ANALYSIS

#### A. Raytheon

A total of thirty devices were purchased for the reliability evaluation. Of these, fifteen were subjected to temperature accelerated life testing. Of these, seven failed non-

TABLE I  
TIME TO FAILURE RAYTHEON LNC 832D DEVICES WHICH FAILED CATASTROPHICALLY

CHANNEL TEMPERATURE (°C)	TIME TO FAILURE (hours)
137	185
162	41
166	42
168	180
184	140
195	48
197	566

(An additional device failed after a few minutes while temperature was being raised to begin the accelerated life test.)

catastrophically (gradual degradation) and eight failed catastrophically (abruptly). Both noncatastrophic and catastrophic failures manifested themselves by an increase in gate resistance. Devices which failed catastrophically exhibited little or no power output after failure but did not “burn out”. As shown in Table I, for the catastrophic failures, there is no correlation between test temperature and time to failure. To date, the best device tested survived for slightly over 2000 h at a 160°C channel temperature. Another device survived for 1340 h at a channel temperature of 193°C. This is substantially better than any results obtained at NRL for Al gate devices with direct connections to Au wires. The data for the seven devices which failed noncatastrophically is summarized in Fig. 2. The data points at 158°C and 192°C represent “MTTF’s” for 2 and 3 devices, respectively. Other data points are time to failure for 1 device each. From Fig. 2 a very rough estimate of the “MTTF” at 125°C channel temperature is  $10^4$ – $10^5$  h. Obviously, the test sample is much too small to reliably extrapolate to room temperature; hence, the quotation marks around MTTF above. It is our philosophy that the exact MTTF is not very important for low MTTF devices, but that an understanding of the failure mechanism is very important. On the other hand, the failure mechanism may not be important for a device with a very large MTTF.

The only significant change in the dc characteristics after stress testing was in the forward gate diode characteristics.

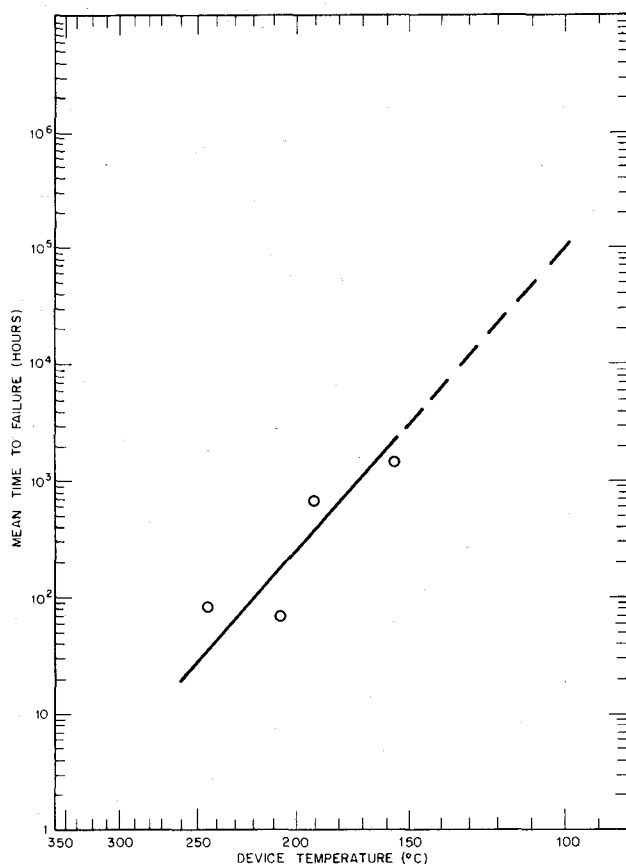


Fig. 2. MTTF versus device temperature for Raytheon LNC 832D devices evaluated at NRL.

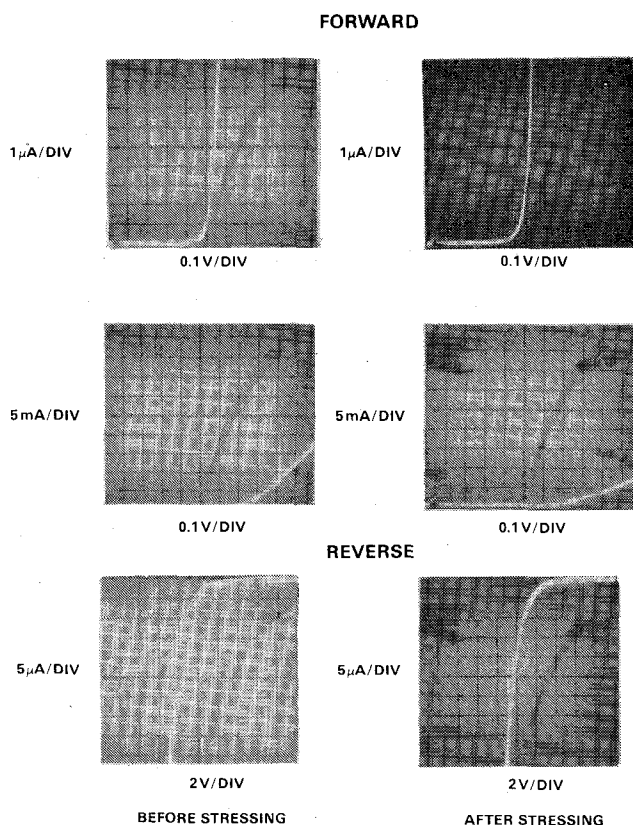


Fig. 3. Forward and reverse  $I$ - $V$  characteristics of a typical Raytheon LNC 832D device.

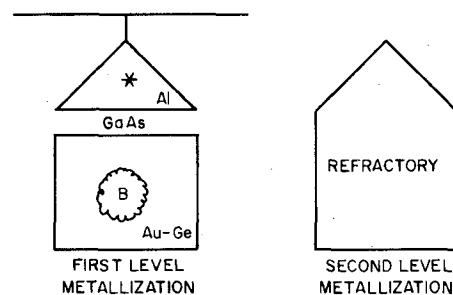


Fig. 4. Schematic of the gate-pad metallization system.

Other characteristics remained virtually unchanged or showed only slight changes. For example, the reverse biased dc gate leakage current at room temperature remained on the order of a few microamperes after stressing. During RF operation, the average gate current usually varied with time (although not in a predictable manner from sample to sample) and typically was on the order of 0.1 mA at room temperature and several tenths of a milliwatt at elevated temperatures. Fig. 3 shows the before and after gate-source  $I$ - $V$  characteristics for a typical device. It is obvious that gate resistance has increased substantially. Some samples were rejected *before* accelerated stressing because their gate resistance was so high that virtually no RF power output could be obtained at 8 GHz.

Devices were examined using a scanning electron microscope (SEM) (in one case both before and after stress testing) but no physical cause of failure was observed at the surface of the devices. However, it seemed apparent that the increase in gate resistance was related in some way to the Al refractory Au "link" (see Fig. 4) on the gate pad. Figs. 5(a)–5(c), respectively, show the device  $I$ - $V$  characteristics before stressing, immediately after failure and several months later. At the suggestion of a scientist from the manufacturer [6], a probe was connected directly to the area marked \* on Fig. 4. The forward  $I$ - $V$  characteristics improved dramatically as shown in Fig. 5(d). Moreover, the improvement remained even after the probe was removed from the \* area in Fig. 4 and reconnected to the device gate lead (Fig. 5(e)). One device was then retested for 168 h at a 120°C base-plate temperature in the RF test setup to see if power output had been restored to its original value. It was found that the initial RF performance was virtually identical to that observed when the device was originally tested. After the elevated temperature test, the device was cooled to room temperature for evaluation. The RF power output had decreased about 0.5 dB. When reexamined on the curve tracer, the forward  $I$ - $V$  characteristics had once again degraded (Fig. 5(f)), although not as badly as immediately after the original RF stress test. This shows that the problem is a high resistance associated with the link. A possible explanation was that this high resistance resulted from  $\text{Al}_2\text{O}_3$  between the Al and the refractory gate metal. However, this hypothesis was ruled out by the following experiment. The forward characteristics of several new device samples were markedly improved by an  $\text{N}_2$  bake at 200–210°C for 150 h as shown in Fig. 6. Since  $\text{Al}_2\text{O}_3$  is not expected to dissociate therm-

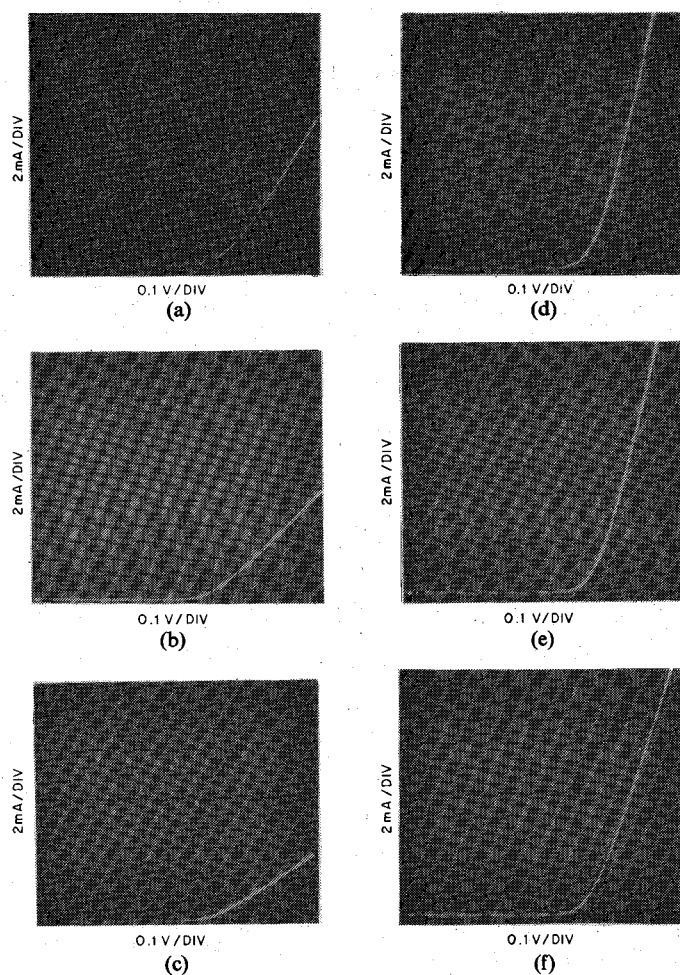


Fig. 5.  $I$ - $V$  characteristics of a Raytheon LNC 832D device. (a) Before temperature stressing. (b) Immediately after stressing. (c) Several months after stressing. (d) With test probe connected directly to the \* area in Fig. 4. (e) With test probe connected to the device gate lead after "punching through" the \* area in Fig. 4. (f) After retesting for 168 h at a 120°C base-plate temperature.

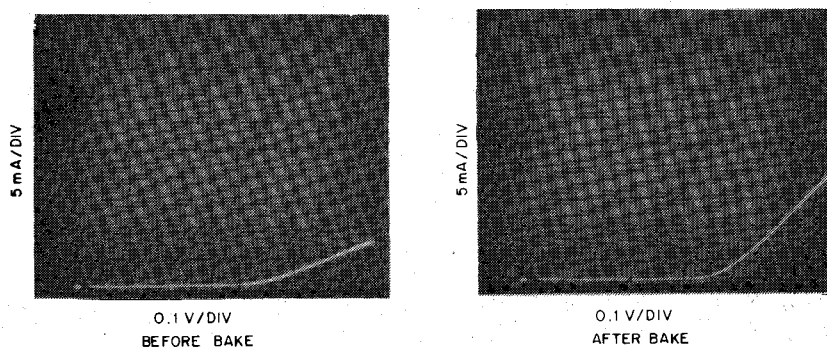


Fig. 6. Forward and reverse characteristics of a typical Raytheon LNC 832D device before and after baking in nitrogen for 150 h at 200–210°C.

ally or undergo chemical reactions with this system at these temperatures, it is ruled out as the source of the high resistance.

A detailed model for the high gate resistance phenomenon should explain the presence of the problem in as-delivered devices, the increase of the gate resistance in

devices tested in ambient and the recovery of device characteristics as a result of the  $N_2$  anneal. The devices were analyzed by microspot Auger electron spectroscopy (AES) and Auger sputter profiling (ASP) in order to identify a failure mode [7], [8]. The results of ASP may be summarized as follows. Significant amounts of oxygen (up to

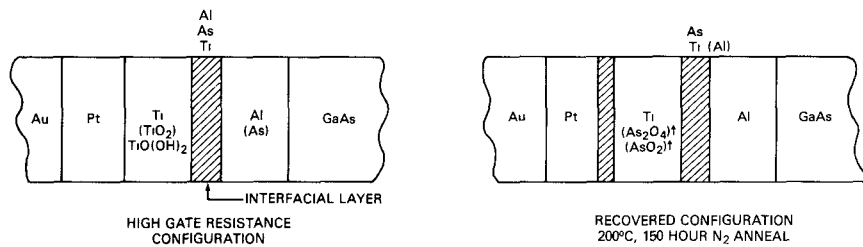


Fig. 7. Schematic summarizing results obtained by Auger sputter depth profiling. (a) Depth profile schematic typical of a degraded device showing possible  $\text{TiO}_2$  and  $\text{TiO}(\text{OH})_2$  in the titanium layer. (b) Depth profile schematic of a typical recovered device.

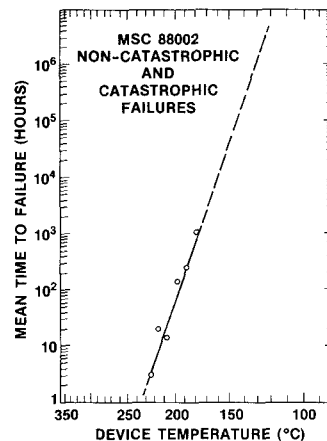


Fig. 8. MTTF versus device temperature for MSC 88002 devices which failed noncatastrophically.

20 atomic percent) were found in the Ti layer of devices with high gate resistance. Arsenic up to 20–25 atomic percent was found in the Al layer of the degraded devices and 3–5 atomic percent in the Al layer of the recovered devices (200–210°C  $\text{N}_2$  anneal). A schematic summarizing the AES profiles is shown in Fig. 7. In the degraded device (Fig. 7(a)) the refractory Ti layer is highly oxidized, while unoxidized Ti is present in the recovered devices (Fig. 7(b)). Thus it is postulated that an oxide or possible hydroxide of Ti ( $\text{TiO}_2$  and  $\text{TiO}(\text{OH})_2$ ) is responsible for the high gate resistance and that this oxide is reduced under  $\text{N}_2$  annealing by the arsenic which has outdiffused from the Al. Enthalpy data for these processes [9] suggest that these reducing and oxidizing reactions can take place at relatively low temperatures (150–200°C). A more detailed explanation will be published in the near future.

#### B. Microwave Semiconductor Corporation (MSC) Devices

A total of twenty-two devices were tested from four different lots [4]. Of these, nine failed catastrophically, three did not fail before testing was terminated and ten degraded to failure gracefully. For the MSC devices, catastrophic failures usually manifested themselves by “burnout”. In this case, the damage to the device is so great that it is not possible to determine the primary failure

mechanism. MTTF as a function of device temperature for devices which failed noncatastrophically is shown in Fig. 8. In Fig. 8, the data point at 190°C represents the MTTF of four devices, the data point at 218°C represents the MTTF of two devices and other data points represent the time to failure of one device each.

From Fig. 8, a MTTF of approximately  $5 \times 10^6$  h is projected for a channel temperature of 125°C. It is not customary to include both catastrophic and noncatastrophic failures on the same MTTF plot. However, it is interesting to note that the slope of Fig. 8 (for noncatastrophic failures only) would be virtually unchanged if the catastrophic failures were included.

The activation energy calculated from Fig. 8 is approximately 2.3 eV. It is recognized that this is very high and that the sample size is relatively small. However, it approaches the value reported by Drukier and Silcox [10] for similar devices tested under dc bias only. Similar MTTF projections were made by Drukier and Silcox [10], [11] from their experiments which were performed under dc bias only.

In contrast to the aluminum gate devices discussed in this paper, the Ti–W–Au gate devices which failed noncatastrophically always demonstrated a dramatic increase in reverse current at low reverse bias voltage. Forward

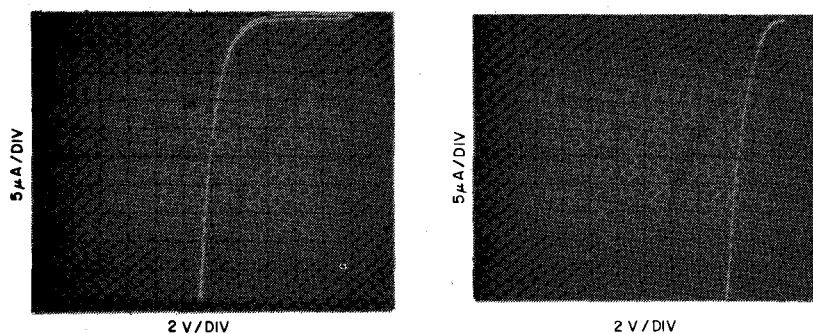


Fig. 9. Reverse characteristics of a typical MSC 88002 device before (left) and after (right) failure caused by accelerated temperature stress testing.

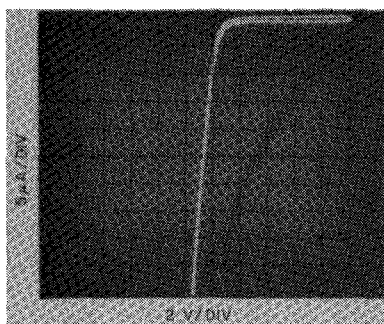


Fig. 10. Improvement in reverse characteristics of the device of Fig. 9 achieved by applying an etch to the device surface.

characteristics including drain-source current at zero gate bias changed relatively little. During RF operation at elevated temperature, average gate current often remained constant at a few milliamperes for some time but always decreased substantially before failure (sometimes changing sign). Fig. 9 shows the change in gate-source diode characteristics for a typical device. Initial attempts to determine the physical mechanism for the failure of these devices proved unsuccessful. These included assessments of device gate-source capacitance before and after testing (which showed virtually no meaningful change) and anneal treatments in vacuum at 200°C for 24 h. Several devices were also examined with an SEM using both conventional and electron beam induced current (EBIC) modes of operation. No gate voids were observed and there was no evidence of electromigration or balling.

However, dc reverse  $I$ - $V$  characteristics of the gate-source diode were dramatically improved by applying an etch to the device surface, consisting of 40 ml of  $H_2O$ , 10 ml of  $HCl$ , 10 ml of  $HF$ , and 5 drops of  $H_2O_2$  for about 5 s. (This etch does *not* strongly attack GaAs.) This was followed by an  $H_2O$  rinse, acetone rinse and blow dry in warm  $N_2$ . Fig. 10 shows the  $I$ - $V$  characteristics after the etch was applied to the same device as that with the characteristics given in Fig. 9. Note that the characteristics are actually slightly better than they were before the stress test. This indicates that surface contamination is responsi-

ble for the noncatastrophic failure of the Au-refractory gate FET's. It is significant that these devices are not passivated.

## V. CONCLUSIONS

The MSC device is the most reliable of the three types of GaAs FET's that NRL has tested to date. The MSC failures we observed are due to surface contamination. These devices were tested unlidded and it might be hypothesized that failure would not have occurred with packaged devices. However: 1) it is not at all clear that packaged devices of this type were or are hermetically sealed; 2) hermeticity is not, in general, a cure for surface contamination since the device chips are always exposed to ambient conditions before packaging; and 3) there are many applications in which an unpackaged chip is required. Passivation of this device may be difficult, but this appears to be the only practical solution of the contamination problem.

Ironically, the Raytheon device fails, at the "link," a structure which appears to successfully solve the void problem. The link problem can almost certainly be solved. Thus the intrinsic reliability of this structure has yet to be determined. A study of Al gate power GaAs FET's [12] manufactured by another laboratory resulted in projections of considerably longer median life. Thus, there is no reason to believe that aluminum gate power GaAs FET's with a

suitable refractory barrier between the gate pad and Au bond wire are inherently unreliable.

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## Single-Frequency Analysis of Radial and Planar Amplifier Combiner Circuits

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**Abstract**—A single-frequency analysis of radial and planar amplifier combiner circuits is presented and expresses the dependence of amplifier combiner performance on the scattering parameters of the amplifiers and combiner/divider networks. The analysis results in useful design

guidelines to achieve optimum performance for small variations in amplifier parameters and graceful degradation under the condition of amplifier failure. Several examples are presented to verify the accuracy of the derived expressions. The scattering matrices of radial and planar combiner/divider networks are derived in the Appendix.

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#### I. INTRODUCTION

THE growing need for solid-state power generation at microwave frequencies has necessitated the development of amplifier combiner circuits to overcome the output